

Barcelona vs Penryn

New AMD CPU Core vs New Intel Semicon Process

Product And Market Share Implications

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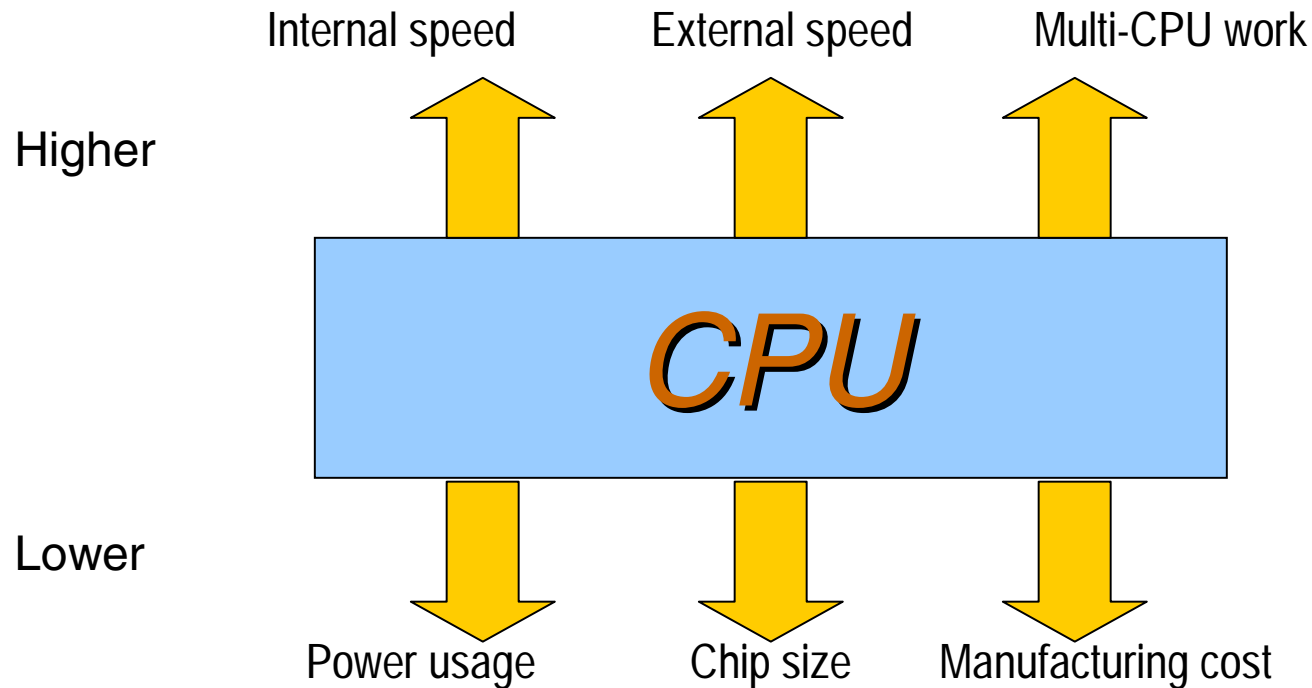
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Agenda

- Intel-AMD market share CY1Q2007 update
- Core 2 market success & AMD response
- Barcelona: Inflection Point for AMD
- Features and market implications
- Intel Penryn: Barcelona spoiler
- Competitive features / implications comparison
- Diagrams
- Timelines
- Futures – 2008 and beyond
- Summary

Technical Must-do's for Successful CPUs



REVISITED: Intel & AMD sides are opposed here vs a year ago

Intel Core 2 – 2006 runaway success

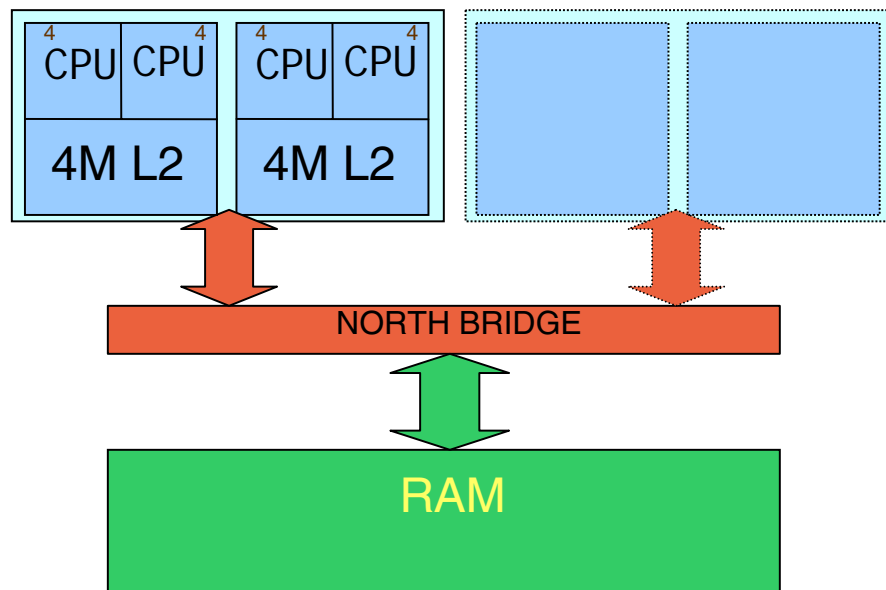
- **Intel's fastest product ramp up in history**
 - 5 M dual-cores within 60 days of announcement
 - Over a million quad-core processors to be shipped by CY2H07
- **Performance leader across key market segments**
 - Desktop, mobile, many workstation & server apps
 - Office, gaming, multimedia, Net apps
 - Exception: memory-bound apps, where AMD still holds an edge
 - Same for 4-socket servers, as Tigerton/Caneland only out CY3Q2007
- **Semicon process advantage used to its best**
 - **Smaller Die, higher speed and lower cost**
 - **Faster Front Side Bus or FSB (often pushed beyond FSB1600 in production end user systems)**
 - **Helps counter AMD memory controller advantage to some extent**

AMD – Urgent Response Needed

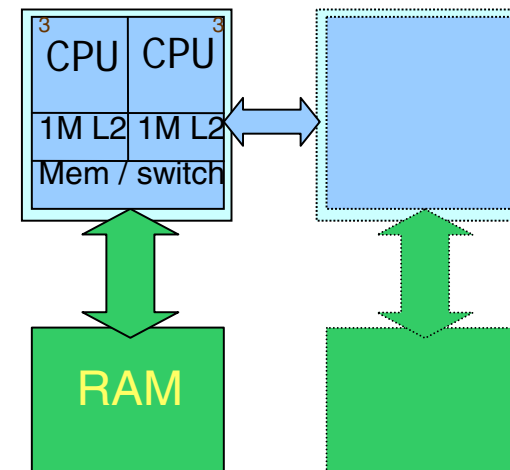
- **Current crop of AMD CPUs is behind on performance**
 - Clock-for-clock, slower in most cases
 - Higher power consumption, even for their early 65 nm parts
 - Their process still needs tuning to get the speed and power usage fixed
 - HyperTransport and integrated memory controller are the only scaling advantages
- **Enormous price pressure leads to radical moves**
 - Aggressive actions aimed at re-gaining market share leadership resulted in a painful price war
 - ATI acquisition and significant capex commitment is leading to a significant cash burn, which AMD can't afford
 - AMD 4x4 dual dual-core desktop: a low-volume emergency fix
- **(Con)FUSION**
 - Fusion between CPU and GPU (board-level, then chip-level) the strategic goal
 - Right now, it likely messes up the overall product roadmap / direction:
 - More CPU cores/chip? Mix CPU / GPU on a chip? What target markets?

Intel / AMD CPU comparison 1 May 2007

INTEL Core 2 / Xeon



AMD Athlon 64 / Opteron



*AMD has faster memory system & interconnect, at the expense of uniformity
Intel has more cores, larger caches, and more instructions per clock (4 vs 3)*

Barcelona – AMD's Survival Matchpoint

- **AMD has to show determination to retake the performance lead**
 - Original K9 & K10 projects were cancelled
 - AMD remained too complacent and was taken aback with Intel's performance overtake by Core 2
- **AMD needs to reassure its users and channels**
 - They had a strong following in both categories for a long time, supporting them during the tough “underdog” days
 - When Athlon64 platform took off with large vendors, those early partners were de-emphasized
 - After such an experience, many early AMD adopters & channels went to Intel
 - If there is no performance lead retake – and ability to ship in volumes – AMD is not likely to get them back again
- **Watershed point**
 - If this new platform fails on the performance and/or delivery fronts, Intel will find it easy to step ahead of the weakened AMD
 - Successful Barcelona ramp is likely “to be or not to be” for AMD

Barcelona features and impacts

- **The first 65 nm process native quad-core single die for X86**
 - Fully optimized for native 4-core operation and inter-core communication
 - Twice the estimated transistor count of Intel Penryn
 - Barcelona – 2-socket workstation & server for mid-CY3Q2007 (4-socket server later?)
 - AgenaFX – 1-socket high-end desktop aimed at CY4Q2007
- **Claimed to be the new performance leader**
 - Twice the floating point (FP) throughput plus slight integer improvements
 - 30% faster memory controller & DDR2 support (desktop)
 - Faster HyperTransport (HT) links
- **Redesigned internal structure**
 - Four cores, each with decreased cache (2x32K L1, 512K L2), communicate through shared 2 MB L3 cache
 - Only one port through L3 to the internal switch for DRAM and HyperTransport
 - More scalable, but also more complex and larger die size, therefore...
 - Harder to optimize for faster clocks, also potential yield problems

Barcelona performance hopes

- **Floating point lead regain**

- AMD was well above Intel X86 for 5 years here, until Core 2 came along
- Critical to bring back technical users, former backbone of AMD success
- Hoping to be up to 30% faster than quad-core Intel in floating point intensive apps

- **Match Core 2 in general purpose performance**

- Integer computation performance lift critical for operating system and office apps
- Also important for future mobile versions

- **Keeping the memory and SMP scalability advantage**

- 30% DRAM speed improvement in desktop version (DDR2-1066)
- Faster HyperTransport for more efficient 4-socket and 8-socket SMP
- All four cores on one die provide full-speed intercore comms, compared to going over the Front Side Bus for cores from different dies on Intel quad-core

Note: SMP stands for Symmetric Multi Processing

Penryn – Intel's 2007 Flagship

- **Improved Core 2, ported to 45 nm process**
 - 20% faster transistors, and brand new type at that
 - Somewhat lower power consumption, even at 20% higher speed
 - Very small die – 107mm² for 410 M transistors
- **Rapid spread across desktop, server and mobile lines**
 - Server, workstation, and high-end desktop volumes by early CY4Q2007
 - Mobile, volumes in CY1Q2008
 - Currently, full stable demo systems in all 3 categories
 - Wolfdale 2-core single-die and Yorkfield 4-core PC / Harpertown 4-core 2-socket dual-die versions available simultaneously
- **New chipset platforms, Penryn-ready & optimized, 2 quarters before**
 - P35 and X38 for mid and high-end desktop
 - Stoakley (Seaburg chipset) for 2-socket server and workstation
 - Caneland for 4-socket server
 - Santa Rosa for mobile

Penryn features & performance

- **Clock-for-clock improvements on floating pt, memory and virtualization**
 - SSE4 instructions, double-speed divider, and super shuffle engine
 - Up to twice the floating point performance on some multimedia and 3-D tasks
 - 50% larger L2 cache – 6 MB per dual-core, plus memory access speedups
 - Up to 75% faster virtual environment switching
- **Plus faster clocks**
 - Starts at 3.33GHz / FSB 1333 for desktop, & 3.2 GHz / FSB 1600 for 2-socket
 - Headroom for faster bins early if AMD's competing CPU speeds require so
 - Expected to reach 3.6 – 3.8 GHz by CY2Q2008
 - 2-core single-die and 4-core dual-die speeds about identical from Day 1
 - ... yet, more low-power optimizations for idle use
- **Initial benchmarks stand by the claims**
 - Between 20% and 50% observed application and benchmark improvements
 - Far more than the clock speed increase alone
 - Seen across the board for both business and (higher) technical / gaming use
 - Expected to increase further as more SSE4 software optimizations come

Competitive position - scenarios

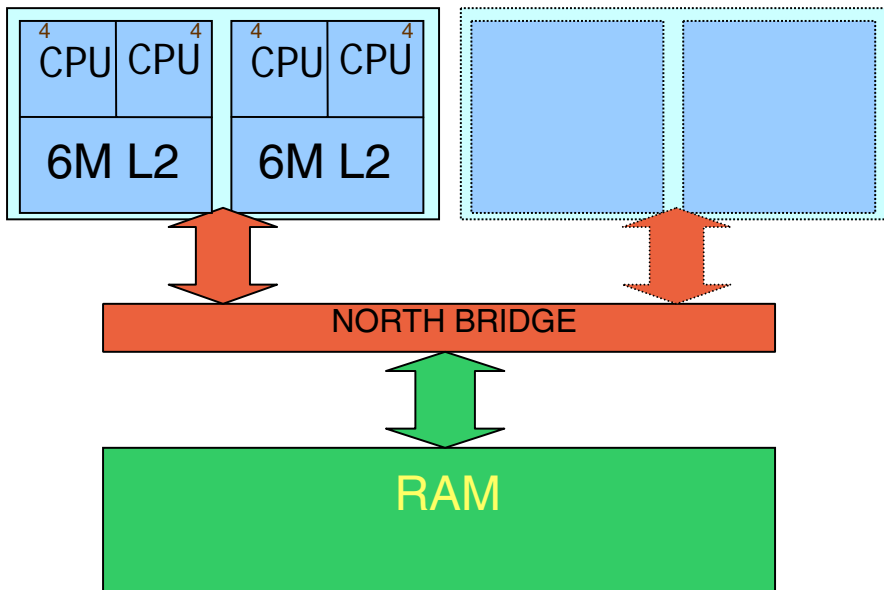
- **1 – Barcelona comes out at planned 2.5 GHz 4-core speed, while Penryn comes out at 3.33 GHz 4-core speed, both with performance as promised**
 - Penryn would be 20% - 40% faster in general-purpose apps
 - Between equal and 20% faster in floating pt (technical, multimedia, game) apps
 - Between equal and 20% slower in very memory-bound apps
 - Between 20% faster and 10% slower for interthread-comm intensive apps

- **2 – Barcelona comes out at higher ~2.7 GHz 4-core speed, while Penryn comes out at 3.33 GHz 4-core speed as default**
 - Closer match in general-purpose apps but Barcelona sees some lead in floating pt
 - Barcelona likely wins in memory bound & thread-comm apps

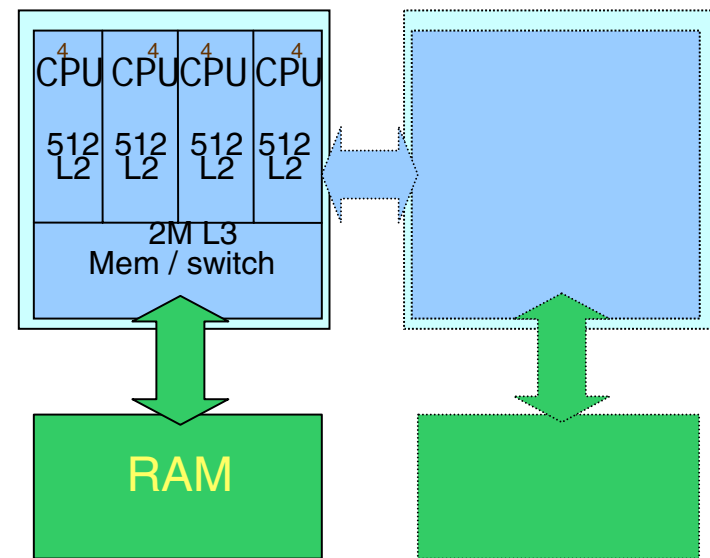
- **3 – Barcelona comes out at 2.5 GHz 4-core speed, while Penryn comes out at higher 3.6 GHz 4-core speed**
 - No contest for most, if not all, general purpose and floating pt apps
 - With Front Side Bus (FSB) increase and matching faster memory, even memory & thread-comm apps are less of an issue

Intel / AMD CPU comparison 1 Nov 2007

INTEL Penryn



AMD Barcelona



AMD: 2X cores/die, equal cores/package, still faster overall interconnect

Intel: 35% faster clocks (4-core), larger common cache, improved FSB / RAM

Nehalem – The 2008 story

- **Next major CPU core revision – Core 3 family?**
 - Core 2 base, but massive microarchitecture & execution rework / speedup
 - Return of HyperThreading in much improved SMT implementation
 - CSI interconnect instead of FSB to match / exceed HyperTransport features
 - Beckton (4 CSI, microbuffer mem) and Gainestown (3 CSI, 3 x DDR3 mem) CPUs
 - Bloomfield desktop (dual-die 8-core?) CPU
 - ... and, yes, 4 cores per die – each core much faster clock-for-clock (Intel)
 - ... and, still somewhat faster clocks
 - Chipsets: Stoutland (4-socket), Tylersburg (2-socket), TBD (1-socket)
- **Simultaneous MultiThreading maximizes thread-rich performance**
 - Many new operating system and application environments are well-threaded
 - New SMT avoids some performance pitfalls of the old HyperThreading
 - 8 threads per 4-core die in 1st Nehalem (16 threads for dual-die 8-core chip)
- **CSI – links with up to 6 neighboring CPU / IO / accelerator devices**
 - Planned to match or exceed HyperTransport 3 in performance
 - Therefore, all Nehalems will have integrated memory controllers
 - DDR3 3+ channel for desktop & 2-socket workstation
 - Microbuffer DIMMs for servers (lower latency & less power vs FB-DIMMs)

Note: SMT stands for Simultaneous MultiThreading; CSI stands for Coherent Scalable Interface

Timelines 2007-2008

- **Intel Penryn launch expected in September, with real volumes in November**
 - Starts also with 2-socket and 1-socket high-end systems
 - Mobile by Feb 2008
 - 1-socket / 2-socket high-end bin slight speed-ups possible ~ Apr 2008
 - 4-socket server by May 2008
- **AMD Barcelona – press samples in May, announcement in June, real volumes in October?**
 - Current information suggests delays till October for reasonable quantities
 - Again, restricted to 2-socket servers, workstations & 1-socket high-end PC systems for this year
 - 4-socket server in CY1Q2008, mobile 4-core may wait for 45 nm in 2009

Timelines 2008-2009

- **Nehalem: Intel's major core revision in CY4Q2008**
 - Also starts with 2-socket and 1-socket high-end systems
 - High-end desktop and 2-socket workstation/server coverage by end-2008
 - Mainstream desktop, mobile and 4-socket server in early 2009
 - 32 nm “Westmere” process shrink expected by CY4Q2009
 - Another 20%-35% performance boost within the same power envelope
- **AMD Shanghai – 45 nm Barcelona successor by mid 2009?**
 - Also expected to be available in dual-die (8 cores total) “Montreal” package
 - In this case, connection via dedicated HT3 link instead of shared front side bus
 - 6 MB L3 cache per 4-core die (12 MB total for Montreal)
 - The first native 4-core mobile unit
 - It could come out earlier if AMD has their 45 nm process up & running

Futures – 2008 and Beyond

● **Early 2008: Tuned-up Penryn vs tuned-up Barcelona**

- A little higher ceiling for Penryn due to smaller die and better process
- AMD may substantially increase CPU / chipset / GPU bundling at this time

● **Late 2008: Nehalem vs further tuned-up Barcelona**

- Expected clear Nehalem win, unless CSI problems surface
- AMD will focus on platform (HT3 speedup, DDR3 memory) improvements
- Lead across whole product line in that case
- **But, limited Nehalem numbers in 2008**
- **Also, new core means unexpected delays possible**
- To buffer for any last-minute Nehalem delays, Intel has to have a Plan B Penryn further tune-up strategy covering at least till early 2009

● **Early 2009: Tuned-up Nehalem vs 45 nm AMD Shanghai**

- Another ~10% Nehalem clock boost at that time
- However, 45 nm Shanghai may receive ~30% add performance
- Race closer, but overall Nehalem will still win
- AMD expected to come out with first Fusion CPU/GPU products by then

Summary

- **Roles reversed from just a year ago, performance-wise, but...**
 - It is a major disadvantage to be the smaller player AND have a slower core
 - Timely, high-speed Barcelona rollout critical for AMD this year
 - By that, I mean full volumes by Oct, or else it will be affected by Penryn
 - Failure would shake up the remaining market confidence in AMD
- **Intel can't remain complacent either**
 - Industry won't let AMD fail, no matter what (IBM etc)
 - Penryn looks good and ready, largely matching or exceeding Barcelona
 - They need to have some volumes by Oct to grab the most of X'mas season
 - Good Nehalem execution in late 2008 would widen their lead
 - If Nehalem delayed, "Plan B" Penryn extra speed-up plan needed till 2009
 - After all, it is a brand new design, so more risks are there than for Penryn

Thank You!

Disclaimer: All points stated should be considered as the Author's subjective opinion, not officially (or in any other way) endorsed by Goldman Sachs or any of the vendors covered in this presentation

Glossary

- **CPU**
 - It is the control unit that processes most of the instructions, therefore the most important part of the computer.
- **FSB**
 - The [bus](#) that connects the [CPU](#) to the chipset (and from there to the [main memory](#)) on the [motherboard](#)
- **Cache**
 - portion of [memory](#) made of high-speed circuits, used to keep the most often accessed [data](#) or [instructions](#) to reduce the accesses to much slower main memory
- **Web pointers for more:**
 - <http://www.mercury-pc.com/glossary.php?id=C>
 - <http://mindprod.com/bgloss/cpu.html>
 - <http://www.itsafe.gov.uk/glossary/cpu.html>